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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS

Case Docket No. 00-255
1496.00039

Washington, D. C. 20231

Date: October 6, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Zhaohui Shen and Daniel Watkins

For: DIAGNOSTIC ARCHITECTURE USING FPGA CORE IN SYSTEM ON A CHIP DESIGN

Enclosed are:

1. X Specification (18 pages); Claims (6 pages); Abstract (1 page)

2. X 6 sheets of formal drawings.

3. X Oath or Declaration Total Pages 3
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to LSI LOGIC CORPORATION, along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$710.00
Total Claims	27	7	x $ 18.00	$126.00
Indep. Claims	2	0	x $ 80.00	$ 0.00
Mult. Dep. Claims			$270.00	$ 0.00

SUB-TOTAL $836.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $876.00

X A check in the amount of $876.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL573625111US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on October 6, 2000.

By: Mary Donna Berkley
Mary Donna Berkley

Respectfully submitted,

By _____
Christopher R. Maiorana
Reg. No. 42,829

Date: October 6, 2000

00-255
1496.00039

DIAGNOSTIC ARCHITECTURE USING FPGA CORE IN SYSTEM ON A CHIP DESIGN

Field of the Invention

The present invention relates to a method and/or architecture for a Field Programmable Gate Array (FPGA) core generally and, more particularly, to a diagnostic method and/or architecture using an FPGA core in a system on a chip (SOC) design.

Background of the Invention

A number of conventional approaches to chip design include (i) directly connecting internal signals to chip I/O pins using multiple layers of multiplexers; (ii) reading on-chip readable registers through host interfaces; (iii) running resistor-transistor logic (RTL) simulations to create special cases to find bugs and verify a fixed solution; and (iv) using emulators to verify the design.

The first conventional approach is limited by the number of the chip I/O pins that can be used to access the internal signals. For example, with 2 layers of 8 to 1 multiplexers, up to

8 signals are needed to be probed simultaneously, totaling 3+3+8=14 I/O pins that are needed for the design. With chip gate counts over 1 million gates, good coverage is difficult to achieve with such an approach.

The second conventional approach can only capture a snap shot of the on-chip readable registers. While such an approach can be helpful in identifying the existence of a bug, it does not offer enough information to precisely locate the bug. Additionally, special effort is needed in the design phase to organize all of the registers.

The third conventional approach can access all the chip internal signals, but has drawbacks. First, such an approach is a software simulation approach that is very time consuming. The simulation speed is usually thousands of times slower than the real system. Second, since such an approach is a software simulation method, it cannot reflect all the factors in the real system. Third, some bugs may not be uncovered with the RTL simulation method because of the running time limitation or the difficulty in creating the simulation case.

The fourth conventional approach can run at a speed up to 1 MHz. However, the emulator is very expensive (i.e., about $1 per

gate). Implementing such an emulator is not easily accomplished. Additionally, the verification cost can be very high.

Therefore, it would be desirable to provide a system for chip design that would minimize the drawbacks associated with conventional systems.

Summary of the Invention

The present invention concerns a system for designing an integrated circuit (IC). The system generally comprising a circuit and a programmable portion used for diagnostics and finding bugs. The circuit generally comprises (i) a functional portion and (ii) a logic portion that may be connected to the functional portion. The logic portion generally includes one or more interfaces. The programmable portion may be configured to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces.

The objects, features and advantages of the present invention include providing a method and/or architecture for implementing a diagnostic architecture using an FPGA core in a system on-chip design that may (i) ease bringing up, verification and debugging by providing interconnection and programming options;

(ii) observe important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the control of the FPGA core; (iv) display appropriate signals on a debugging workstation, allowing many debugging features to be supported such as: (a) triggering and tracing based on internal signals, (b) dynamically changing host register values and (c) providing complex monitoring functions, since the FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a preferred embodiment of the present invention;

FIG. 2 is a more detailed block diagram of the present invention;

FIG. 3 is an even more detailed block diagram of the present invention;

FIG. 4 is a timing diagram illustrating an exemplary operation of the present invention;

FIG. 5 is an example of an implementation of the present invention on a chip; and

FIG. 6 is another implementation of the present invention.

Detailed Description of the Preferred Embodiments

With the exponential increase of the number of transistors integrated on a single chip, diagnostics of the chip becomes more and more challenging. Better accessibility to internal signals of the chip is highly demanded.

The present invention implements an FPGA core as an embedded Field Programmable Gate Array core that may be used to enable logic to be programmed after the silicon has been produced. The FPGA core can be used to implement on-chip diagnostics to enable debugging functions, such as bus monitoring, probing, single step running, triggering, capturing, etc. One example of such an FPGA may be found in co-pending application Serial No. 09/464,741, which is hereby incorporated by reference in its entirety.

Referring to FIG. 1, a diagram of a system 100 is shown in accordance with the preferred embodiment of the present invention. The system 100 generally comprises an FPGA core and logic block (or circuit) 102 and a debugging workstation block (or circuit) 104. The circuit 102 may be implemented as a single chip or integrated circuit (IC). Additionally, the debugging workstation 104 generally works in combination with the FPGA core and logic block 102.

The system 100 generally allows for design of an integrated circuit (IC). The circuit 102 generally comprises a functional portion that varies with design and a logic portion connected to the functional portion (to be discussed in connection with FIGS. 2 and 3). The logic portion generally includes one or more interfaces that may be coupled to the debugging circuit 104. The debugging circuit 104 may be configured to detect errors in the logic portion through the one or more interfaces.

Referring to FIG. 2, a more detailed block diagram of the FPGA core and logic block 102 is shown. The FPGA core and logic block 102 generally comprises a register portion 110, a logic portion 112, a register portion 114, an FPGA core portion 116 and a control portion 118. The FPGA core 116 may be implemented to

control the chip 102. The register portion 110 generally comprises a number of register blocks 120a-120n. The register portion 114 generally comprises a number of register blocks 122a-122n. The logic block 112 generally comprises a combinational logic block (or circuit) 130, an I/O block (or circuit) 132 and a multiplexer circuit 134. A particular implementation of the multiplexer 134 may be varied in order to meet the criteria of a particular implementation.

The register block 110 may communicate with the FPGA core 116 through a bus 140 and a bus 142. Similarly, the register block 114 may also communicate with the FPGA core 116 through a bus 144 and a bus 146. The buses 140, 142, 144 and 146 may be implemented, in one example, as multi-bit buses. However, the buses 140, 142, 144 and 146 may also be implemented as single bit buses, if appropriate. Additionally, the buses 140, 142, 144 and 146 may also be implemented as bidirectional buses.

The FPGA core 116 may also communicate with the control block 118 through a bus 148. The FPGA core 116 may communicate through a number of I/O pins (e.g., I/O_PINS) over a bus 150. The FPGA core 116 may also communicate with the debugging workstation 104 through a bus 152. The buses 148, 150 and 152 may be

implemented as single bit buses or multi-bit buses. Additionally, the buses 148, 150 and 152 may be implemented as bidirectional buses.

The system 100 may provide a chip diagnostics architecture by implementing the FPGA core 116. By using the FPGA core 116 to implement such chip diagnostics, simultaneous probing of internal signals can be achieved while the system 100 is running under predetermined conditions (e.g., a normal mode of operation). Additionally, a process may be implemented to allow the FPGA core 116 to collect data from the registers 120a-120n and 122a-122n using a scan chain, while the system 100 is running under predetermined conditions (e.g., a step mode configuration) controlled by the FPGA core 116.

With the FPGA core 116 running at a speed much faster than a clock of the system 100, data collecting from the internal signals can be done while the system 100 is running in the normal mode. For example, in consumer products, devices typically only run at 27 MHz, while the FPGA core 116 can operate at as fast as 200 MHz to 400 MHz, or even higher. The FPGA core 116 can be programed to simultaneously probe multiple internal signals that are connected to the I/O block 132 while the system 100 is running

at a normal operational speed. After the data is collected and compressed, the data will be sent to the debugging workstation 104. The waveforms of the internal signals under probing can be displayed as if they are directly connected to a logic analyzer by internal wires (via the debugging workstation 104).

The FPGA core 116 may be implemented to support up to 1K of I/O data. Therefore, up to 1K of internal signal probing can be supported simply by directly connecting the signals to the I/O_PINS of the FPGA core 116. Multiplexing (e.g., through the multiplexer 134) may also be implemented to increase an amount of I/O data. For example, if 2 layers of 8 to 1 multiplexers are used, up to 64K of internal signal probing may be supported. Additionally, multiplexers may allow the circuit 100 to drastically reduce the number of internal connection wires. The particular number of I/Os supported by the FPGA core 116 as well as the particular number of multiplexers may be varied to meet the design criteria of a particular implementation.

By controlling the system clock, the FPGA core 116 may also be programed to run the system 100 in a single step mode. By utilizing the scan chain under the single step mode, the FPGA core 116 may collect data from the register blocks 110 and 114

implemented on the system 100. Since the scan chain is usually very long (e.g., several thousands of registers per scan chain), the scan chain may be separated into small segments to speed up data collection.

Referring to FIG. 3, a diagram illustrating the breaking of a scan chain into segments is shown. The scan chain implementation of the circuit 102 generally comprises a multiplexer logic block (or circuit) 160 and a scan chain segment block (or circuit) 162. The multiplexer logic block 160 generally comprises a number of multiplexers 164a-164n. The scan chain segment block 162 generally comprises a number of multiplexers 166a-166n and a number of scan chain segments (e.g., SCAN_SEG0, SCAN_SEG1 ... SCAN_SEGX). The scan chain segments may allow the FPGA core 116 select and collect register data more quickly.

FIG. 4 shows the timing relationship between a system clock signal (e.g., SYS_CLK) and a clock signal (e.g., DIAG_CLK). The clock signal DIAG_CLK may be implemented as a diagnostic clock. The FPGA core 116 may control the diagnostic clock signal DIAG_CLK. The system clock signal SYS_CLK may be implemented during the normal mode. The diagnostic clock signal DIAG_CLK may be implemented during the single step mode. Both the clock signal

SYS_CLK and the clock signal DIAG_CLK are derived from the FPGA core 116.

The following steps outline collecting of register data using the segmented scan chain under single step mode:

(i) by programming the FPGA core 116, the debug workstation 104 may increase a particular number of registers on the chip 100 that need to be observed as well as the observation start and stop times of the particular registers;

(ii) during the observation start and stop time, the chip 100 may operate under the single step mode;

(iii) the FPGA core 116 generates the clock signal SYS_CLK, the clock signal DIAG_CLK and select signals DIAG_SEL10 and DIAG_SEL11 (which may be multi-bit or single bit signals) to control which scan segments need to be accessed;

(iv) under the single step mode, after each effective edge of the system clock SYS_CLK, the data in the selected scan segments SCAN_SEG0-SCAN_SEGX may be shifted to the FPGA core 116, then shifted back to the selected scan segment SCAN_SEG0-SCAN_SEGX, and then the clock signal SYS_CLK may resume; and

(v) only the data from the registers that needs to be monitored may be stored and compressed. The I/O interface may then transfer the data to the debugging workstation 104.

Referring to FIG. 5, one or more chip I/O pins 200a-200n are shown connected to the FPGA core 116. Such a connection can allow the FPGA core 116 to monitor the I/O of the chip 102. In addition, one of the I/O pins 200a-200n can be connected as an input pin to the FPGA core 116. An internal module from the FPGA core 116 may generate a signal to drive the chip during the chip debugging. With a system on chip design, the signals among different blocks can also be connected through the FPGA core 116. Additionally, the FPGA core 116 can bridge signals between different modules 202a-202n. Such bridging can help in debugging of different modules. Such bridging can also help in isolating problems.

For those modules 202a-202n that are sensitive to the clock frequency, such as the refresh control block in an DRAM/SRAM interface (not shown), the FPGA core 116 can keep these modules running at normal clock speed. However, special attention needs to be paid during the design phase, to make the whole system work

normally while the system clock is slowed down during the step running mode.

Computer Aided Design (CAD) software may also need to be developed for the debugging workstation 104. The debug workstation 104 can be developed to work together with the on-chip FPGA core 116. The functions of the debug workstation include one or more of the following:

(i) programing the FPGA core to implement user required functions,

(ii) collecting data from the FPGA core though the I/O interface, and

(iii) offering an end user interface to the debugging engineer.

One function of such software may be to offer an easy to use interface to the user.

Referring to FIG. 6, a work flow (or system) 300 of an example software is shown. The software will read in the probe name file, in which all the signals that can be probed are logged. The netlist file and the RTL codes of the design are read. All the registers on different scan segments are mapped to the netlist and related to the RTL codes. In this way, the user can easily decide

which signals need to be observed during the debugging period. While the chip 102 is running at normal speed, the software can display any of the internal signals that are connected to the I/O of the FPGA core 116. While the chip 102 is running at single step mode, the software can display all the signals on the chip 102. This is because under single step mode, the FPGA core 116 can be programmed to access any of the on-chip registers. All the combinational signals can be derived from the related register values and the netlist information. By using such software, users can also program the FPGA core 116 to implement different debugging functions. The debugging workstation 104 and the CAD software can be reused in different projects, resulting in reduction of cost.

The function performed by the system 300 of FIG. 6 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate

network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

With the on-chip programming capability of the FPGA core 116 and the debugging software, many new features can be implemented without increasing the cost in diagnostics. Such may include one or more of the following:

(i) programing the FPGA core 116 to dump the host register every N clock cycles,

(ii) capturing signals every N clock cycles,

(iii) dynamically changing the host register values,

(iv) single step tracing, counters and pointers monitoring,

(v) searching for a specific signal pattern,

(vi) tracing an internal state machine triggered on a programmed condition,

(vii) monitoring the correctness of a bus protocol, and/or

(viii) implementing statistics counting to measure the performance (e.g., the active time on bus request, the execution coverage of the internal state machines, etc.).

Individual aspects described can be implemented either alone or in combination. For example, only particularly important signals may need to be connected to the FPGA core 116 for real time monitoring. The present invention may provide a FPGA core in an ASIC architecture that eases chip bring up, verification and debugging by interconnection and programming options. The present invention may allow important signals of a chip to be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. The present invention may allow all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip.

By programming the FPGA core 116, many debugging features can be supported, such as one or more of the following:

(i) programmed triggering and tracing based on internal signals (e.g., tracing the internal state machines, pointers, counters, etc.)

(ii) triggering on the specific values of address, data, or command bus;

(iii) dynamically changing the host register values; and/or

(iv) complex monitoring functions (e.g., protocol monitoring). Additionally, the system 100 may reduce chip debugging/verification time and product time to market.

The FPGA core 116 may simultaneously probe multiple internal signals. By utilizing the scan chain under the single step mode and with the on-chip FPGA core 116 acting as the data process center, all the signals on the chip 102 can be observed. The FPGA core 116 can be used to bridge the signals between different modules, and the under test mode, to isolate a specific module and drive signals to test the specific module. The FPGA core 116 can also be used to add or verify bug fixes. The process of the debugging workstation 104 working with the on-chip FPGA core

116 to generate many powerful debugging features may also be implemented.

The system 100 may provide functionality of a CAD software that may be implemented to work with the diagnostics design. The system 100 may allow for enhanced debugging capabilities with the diagnostics design, such as searching for a specific signal pattern, tracing the internal state machine and/or triggering on a programmed condition. The system 100 may provide on the fly monitoring of the correctness of the bus protocol, doing statistics counting to measure the performance and/or testing coverage.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. A system for designing an integrated circuit (IC) comprising:

a circuit comprising (i) a functional portion and (ii) a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said function portion.

2. The system according to claim 1, wherein said logic portion includes one or more interfaces, and said system further comprises:

a debugging/bug fix circuit configured to detect errors in said logic portion through said one or more interfaces.

3. The system according to claim 1, wherein said system comprises a diagnostic architecture using an FPGA core in a system on a chip design.

4. The system according to claim 2, wherein said system is further configured to (i) provide ease in bringing up, (ii) verification and (iii) debugging, each by interconnecting said circuit and said debugging/bug fix circuit.

5. The system according to claim 1, wherein said system is further configured to provide one or more programming options of said circuit.

6. The system according to claim 2, wherein said system is further configured to allow observation of one or more signals by said debugging/bug fix circuit.

7. The system according to claim 6, wherein said system is further configured to allow observation of said one or more signals when running in a normal mode.

8. The system according to claim 1, wherein said system is further configured to run in a single step mode.

9. The system according to claim 8, wherein said system is further configured to run in said single step mode when controlled by a gate or a core.

10. The system according to claim 9, wherein said core comprises said FPGA core.

11. The system according to claim 9, wherein said core is programmable.

12. The system according to claim 2, wherein said debugging/bug fix circuit comprises a debugging workstation.

13. The system according to claim 2, wherein said debugging/bug fix circuit is further configured to allow one or more debugging features.

14. The system according to claim 13, wherein said one or more debugging features support triggering and tracing based on one or more internal signals.

15. The system according to claim 13, wherein said one or more debugging features support dynamically changing host register values.

16. The system according to claim 13, wherein said one or more debugging features provide complex monitoring functions.

17. The system according to claim 1, wherein said system is further configured to reduce debugging/verification time and/or improve product time to market.

18. The system according to claim 1, wherein said circuit is further configured to operate in a normal mode and a single step mode.

19. The system according to claim 18, wherein said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode is configured to provide a plurality of signals of said functional portion.

20. The system according to claim 18, wherein a scan chain is used to diagnose or fix a bug via the logic portion.

21. The system according to claim 18, wherein the programmable portion is further configured to bridge one or more of said plurality of signals between a plurality of modules.

22. The system according to claim 2, wherein said debugging/bug fix circuit and said circuit are configured to generate one or more debugging features.

23. The system according to claim 2, wherein said debugging/bug fix circuit is configured to work with Computer Aided Design (CAD) software to provide one or more diagnostic functions.

24. The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of searching for a specific signal pattern, tracing the internal state machine, triggering on a programmed condition and other appropriate diagnostic functions.

25. The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implementing statistics counting to measure the performance and the testing coverage.

26. A method for diagnostics comprising the steps of:

(A) interfacing a chip with a core;

(B) presenting one or more internal signals of said chip; and

(C) verifying or fixing bugs in said chip with said one or more internal signals.

27. A computer readable medium configured to store instructions for executing the steps of claim 26.

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ABSTRACT OF THE DISCLOSURE

A system for designing an integrated circuit (IC). The system generally comprising a circuit and a programmable portion used for diagnostics and finding bugs. The circuit generally comprises (i) a functional portion and (ii) a logic portion that may be connected to the functional portion. The logic portion generally includes one or more interfaces. The programmable portion may be configured to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces.

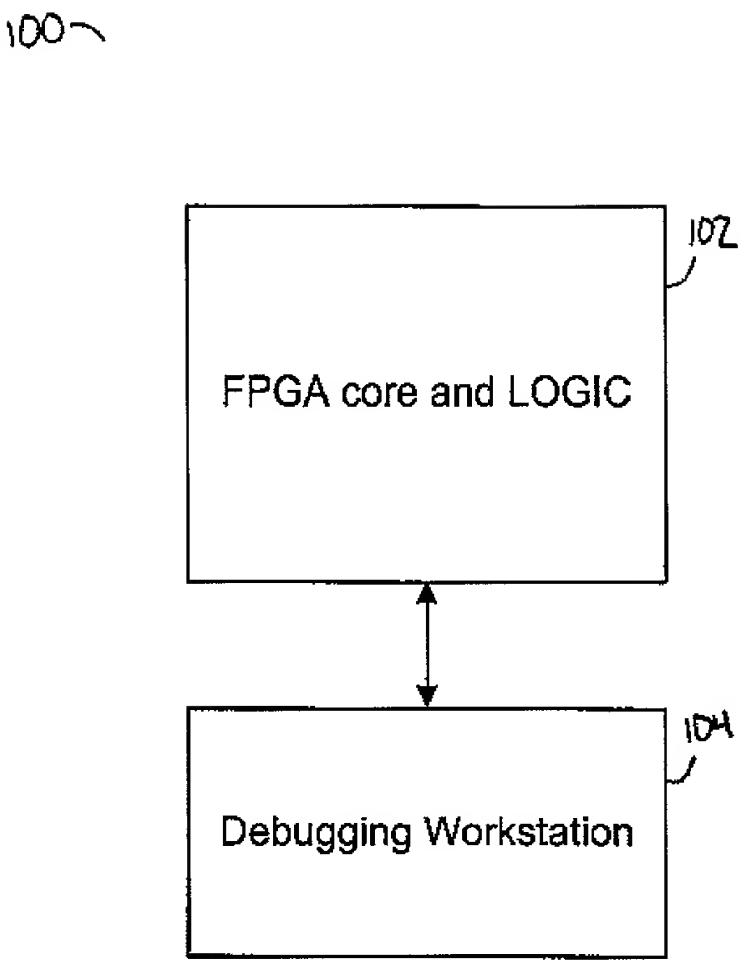
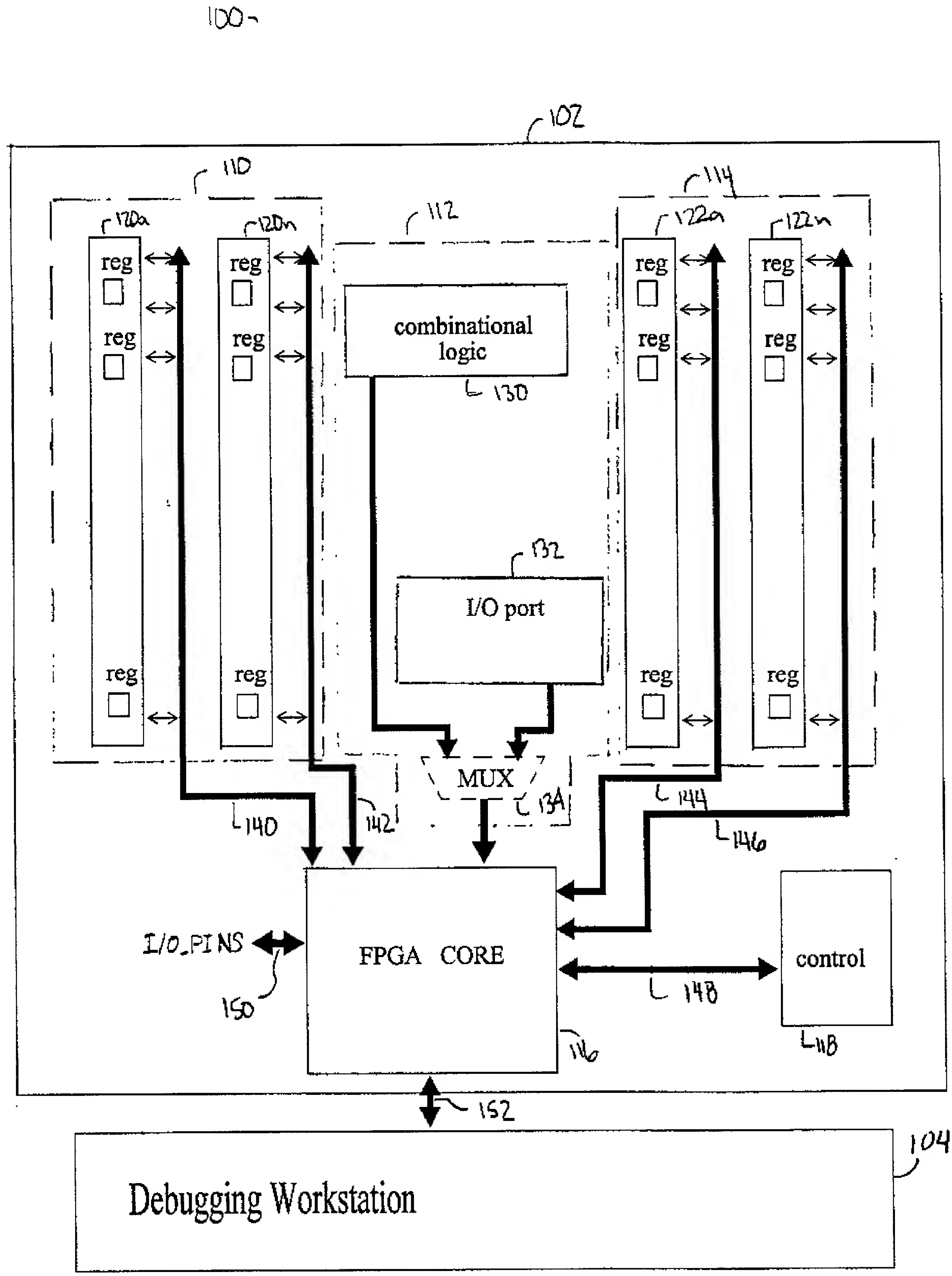


FIG. 1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120n
112
114
122a
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reg
reg
reg
combinational logic
130
132
I/O port
MUX
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FPGA CORE
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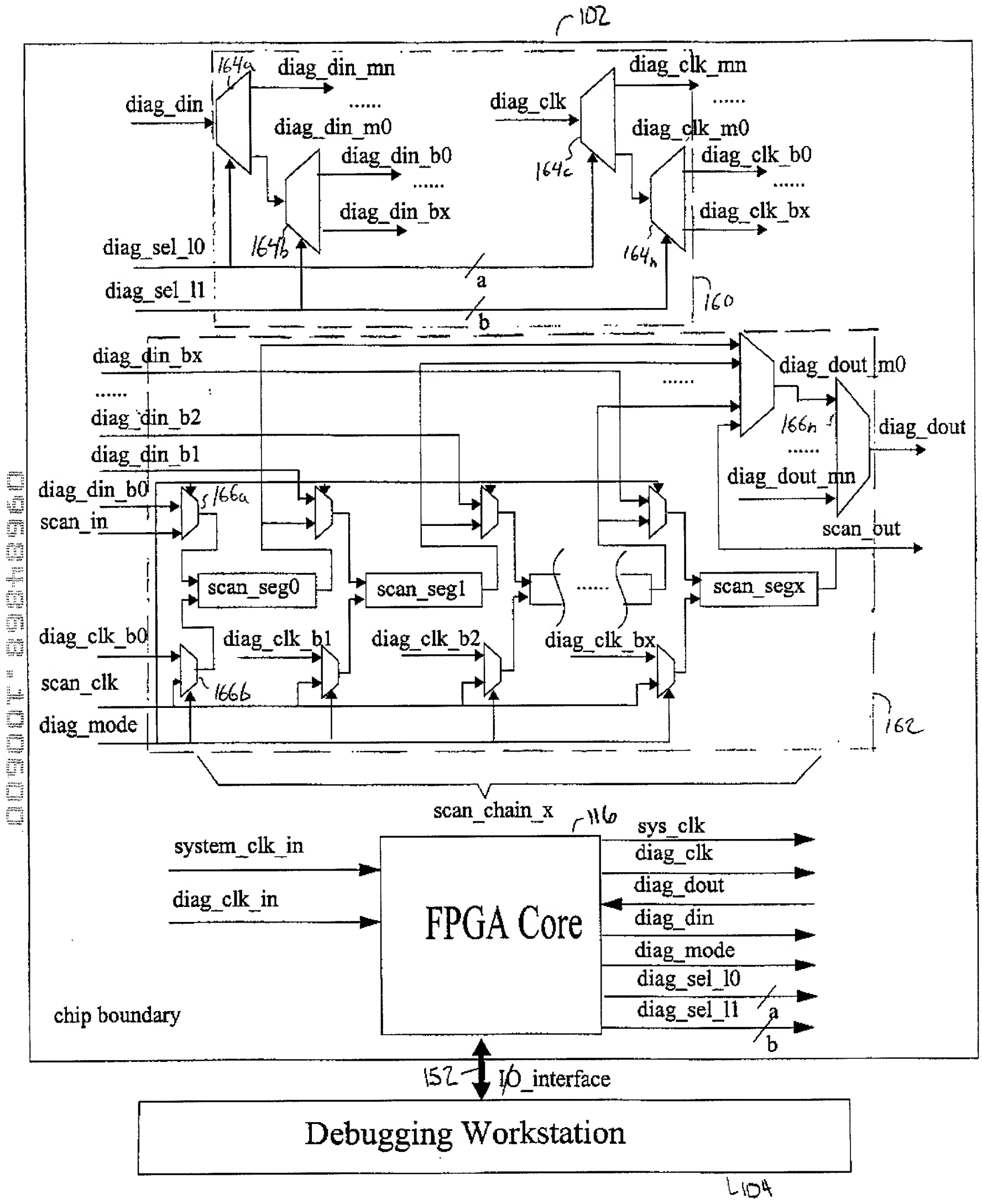
148
150
116
118
152
104
Debugging Workstation

FIG. 2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diag_clk_mn
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diag_clk_bx
diag_sel_l0
diag_sel_l1
a
b
160
diag_dout_m0
diag_dout
diag_dout_mn
scan_out
scan_in
scan_seg0
scan_seg1
scan_segx
diag_clk_b0
diag_clk_b1
diag_clk_b2
diag_clk_bx
scan_clk
diag_mode
162
scan_chain_x
116
system_clk_in
diag_clk_in
FPGA Core
sys_clk
diag_clk
diag_dout
diag_din
diag_mode
diag_sel_l0
diag_sel_l1
chip boundary
152
IO_interface
Debugging Workstation
104

FIG. 3

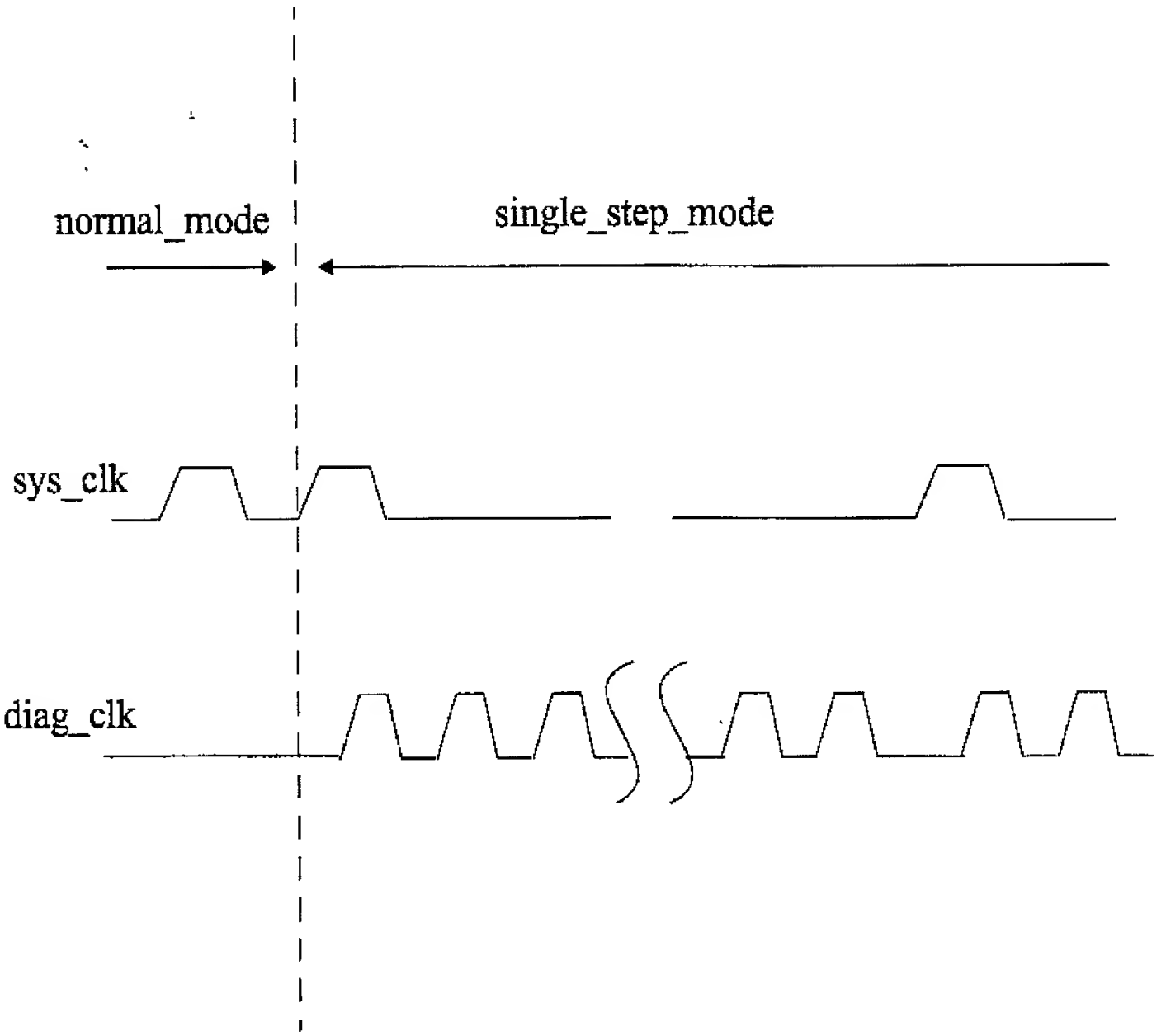

FIG. 4

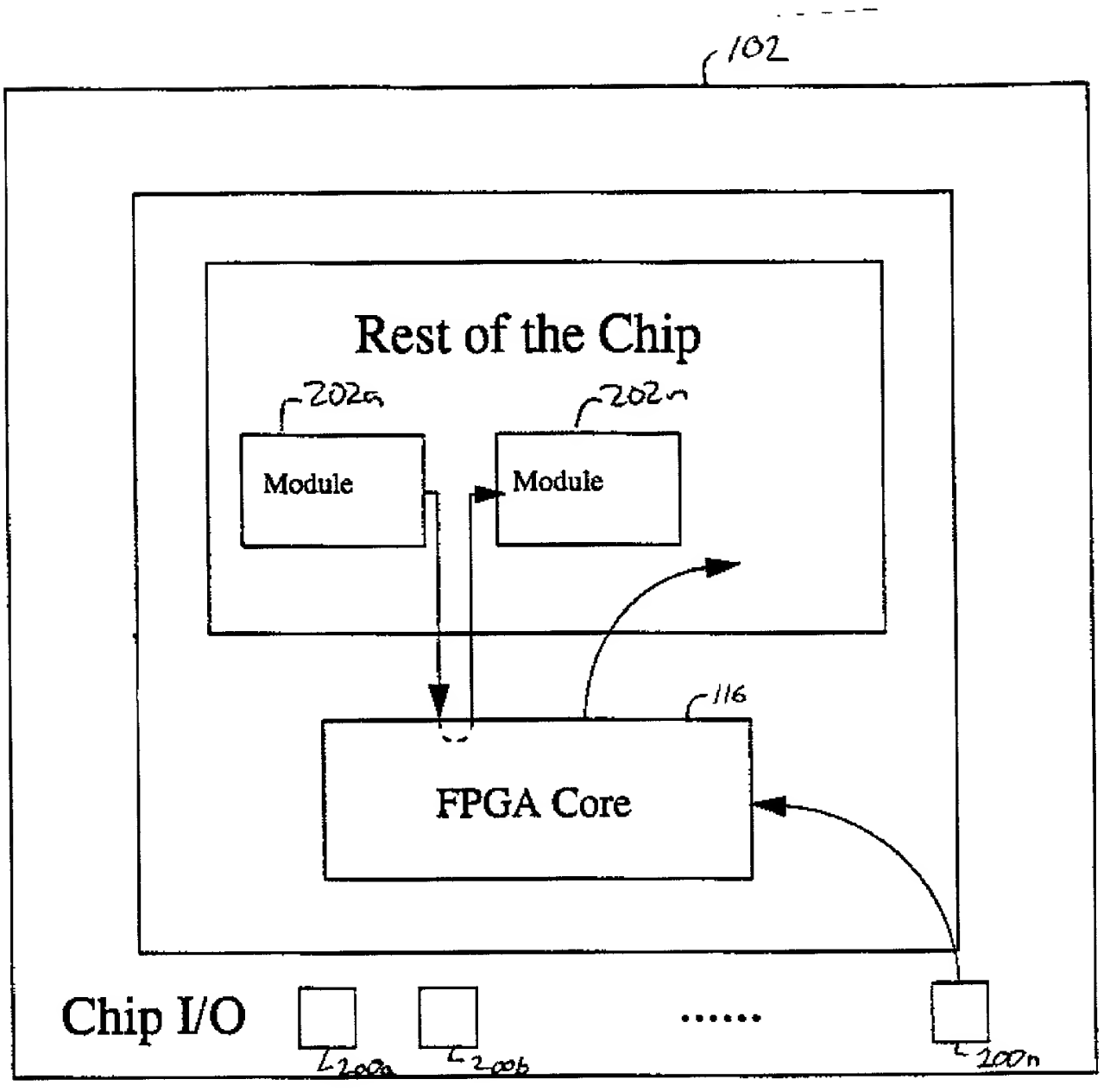
102
Rest of the Chip
202a
202n
Module
Module
116
FPGA Core
Chip I/O
200a
200b
200n

FIG. 5

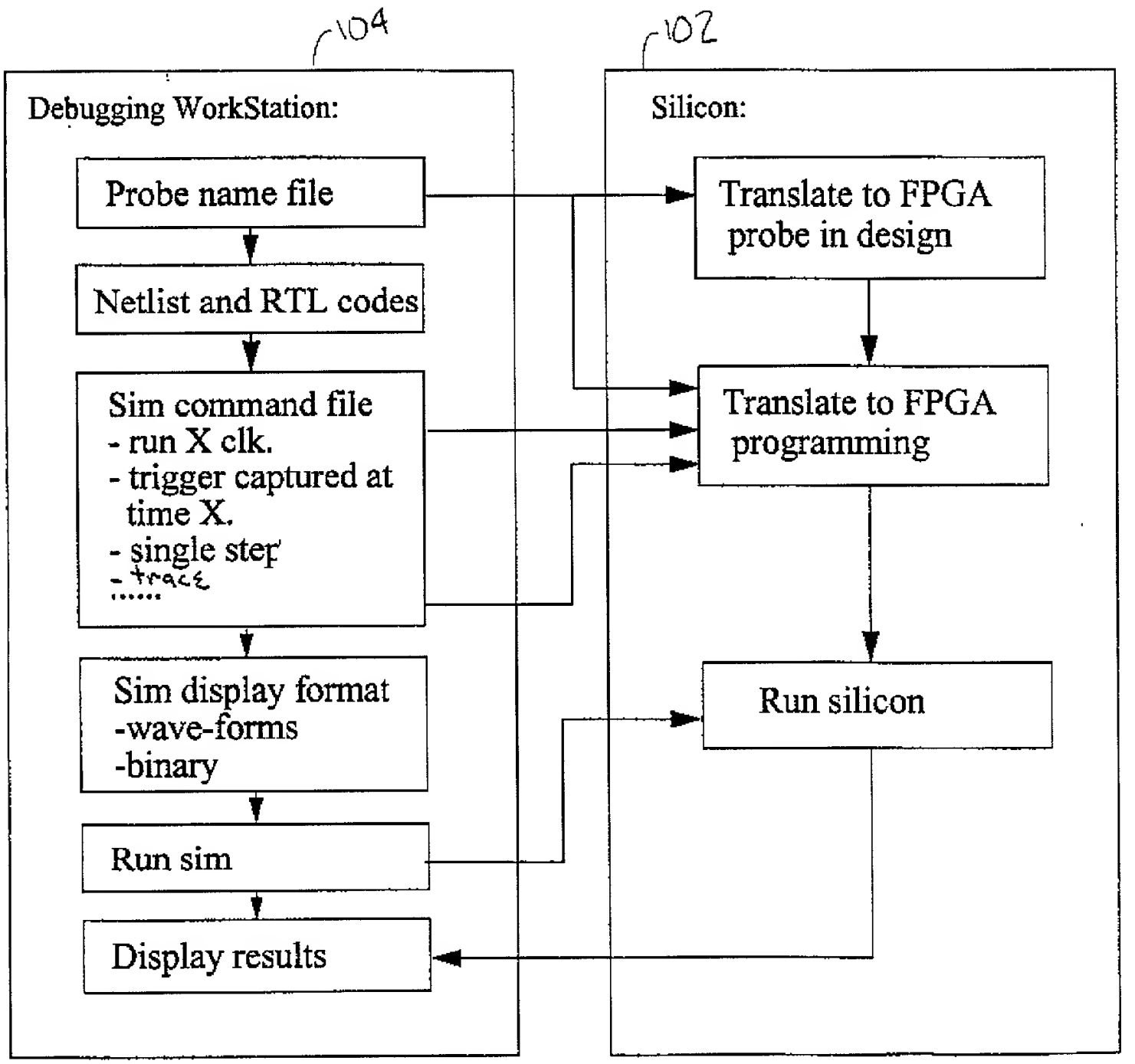
300
104
102
Debugging WorkStation:
Silicon:
Probe name file
Netlist and RTL codes
Sim command file
- run X clk.
- trigger captured at time X.
- single step
- trace
.....
Sim display format
-wave-forms
-binary
Run sim
Display results
Translate to FPGA probe in design
Translate to FPGA programming
Run silicon

FIG. 6

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DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled **"DIAGNOSTIC ARCHITECTURE USING FPGA CORE IN SYSTEM ON A CHIP DESIGN"**, which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or

refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application:

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We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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